CLAIMS

1. A reconfigurable control structure for CPUs, comprising:

a first control unit with a first basic instruction set associated therewith;

a second control unit, with a second instruction set associated therewith; a programming element associated with said second control unit for rendering said second instruction set selectively modifiable; and

at least one circuit element for supplying instruction codes to be executed to said first control unit and to said second control unit, so that each instruction can be executed under the control of at least one between said first control unit and said second control unit according to whether each instruction is comprised within at least one between said first basic instruction set and said second selectively modifiable instruction set.

2. The structure according to claim 1, wherein said at least one circuit element is configured for sending said instruction codes to be executed in a undifferentiated way to said first control unit and said second control unit, and the structure further comprises a selection module configured for recognizing whether the instruction to be executed each time supplied by said at least one circuit element belongs to said first basic instruction set or to said second selectively modifiable instruction set.

3. The structure according to claim 2, further comprising an output module which has:

a first set of input lines connected to an output of said first control unit;

a second set of input lines connected to an output of said second control unit; and

a set of output lines;

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wherein said output module is connected to said selector module for transferring on said set of output lines the signal present on said first set of input lines and on said second set of input lines when said selector module recognizes whether the instruction processed each time by the structure belongs to said first basic instruction set or to said second selectively programmable instruction set.

4.   The structure according to claim 1 wherein said first control unit is configured as a finite state machine that is able to assume an inoperative state and at least one active state for execution of a respective instruction comprised in said first basic instruction set.

5.   The structure according to claim 1 wherein said first control unit is configured as a wired-logic control unit.

6.   The structure according to claim 1 wherein said second control unit is configured as a finite state machine that is able to assume an inoperative state and at least one active state for execution of a respective instruction comprised in second set of selectively modifiable instructions.

7.   The structure according to claim 1 wherein said second control unit is basically configured as a microprogrammed-logic control unit.

8.   The structure according to claim 8, wherein said second control unit is configured as a finite state machine with a memory associated therewith which is able to receive a stored microprogram defining the sequences of the control signals of said finite state machine.

9.   The structure according to claim 1 wherein said first control unit and said second control unit are configured as finite state machines having respective

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numbers of state bits and the number of state bits of said second control unit is greater than or equal to the number of state bits of said first control unit.

10. The structure according to claim 1, wherein:

said first control unit is of a hardwired type; and

said second control unit is programmable, programming of said second control unit being carried out by said first control unit by means of instructions.

11. The structure according to claim 10, wherein programming of said second control unit by said first control unit is carried out by means of an operation of memory programming.

12. The structure according to claim 10 wherein programming of said second control unit by said first control unit is carried out by means of at least one programming instruction included in said first basic instruction set.

13. A process for using a control structure that includes a first control unit with a first basic instruction set associated therewith; a second control unit with a second instruction set associated therewith; a programming element associated with said second control unit for rendering said second instruction set selectively modifiable; and at least one circuit element for supplying instruction codes to be executed to said first control unit and to said second control unit, the process comprising associating with each of said instructions to be executed an operating code that includes at least one bit identifying one between said first control unit and said second control unit designed to generate control signals for the instruction to be executed.

14. The process of claim 13, further comprising programming said second instruction set so that said second instruction set duplicates, at least in part, said first basic instruction set.

15.   The process according to claim 14, further comprising: executing a function for debugging said first control unit and, in the event, in the context of said debugging function, of a given instruction not being implementable in a satisfactory way on said first control unit, implementing on said second control unit said instruction not implementable in a satisfactory way on said first control unit.

16.   The process of claim 13, further comprising receiving programming data at the first control unit which uses the programming data to program the second control unit.

17.   A reconfigurable control structure for CPUs, comprising:

an input for receiving instructions;

an output for presenting control signals produced by execution of the instructions;

a hard-wired control unit coupled between the input and the output and structured to execute a pre-defined set of the instructions into a plurality of the control signals; and

a programmable control unit coupled between the input and the output and structured to execute a programmable set of the instructions, the programmable control unit including a memory that stores definitions of the programmable set of instructions and an execution unit that executes the instructions according to the stored definitions to produce a plurality of the control signals.

18.   The control structure of claim 17, further comprising a selection module coupled to the input and configured to recognize whether each of the instructions received at the input is to be executed by the hard-wired control unit or by the programmable control unit.

19.   The control structure of claim 18, further comprising an output module having a first input connected to an output of the hard-wired control unit, a second input connected to an output of the programmable control unit, an output coupled to the output of the control structure, and a control input coupled to an output of the selection module, the output module being structured to selectively connect the output of the output module to one of the first and second inputs depending which of the control units the selector module recognizes as being appropriate for executing a current one of the instructions received by the selector module.

20.   The control structure of claim 18 wherein the control units have respective state outputs for outputting state information and respective state inputs for receiving state information, the control structure further comprising:

a switching device having first and second inputs coupled respectively to the state outputs of the control units, an output, and a control input coupled to an output of the selector module, the switching device being structured to selectively connect the output of the output module to one of the first and second inputs depending which of the control units the selector module recognizes as being appropriate for executing a current one of the instructions received by the selector module; and

a state register having an input connected to the output of the switching device and an output connected to the state inputs of the control units.

21.   The control structure of claim 17 wherein the hard-wired control unit is configured as a finite state machine that is able to assume an inoperative state and at least one active state for execution of the instructions of the pre-defined set.

22.   The control structure of claim 17 wherein the programmable control unit includes a finite state machine that is able to assume an inoperative state and at least one active state for execution the instructions of the programmable set.

23. The control structure of claim 17 wherein programming of the programmable control unit by the hard-wired control unit is carried out by means of at least one programming instruction included in the pre-defined set of instructions.